Amendments to the Drawings:

Replacement drawings for six sheets including Figures 2, 7-13 and 16-17 have been prepared by a competent draftsman and are included as an appendix. Applicants request that these drawings be substituted for these figures currently on file in the application. No changes have been made to the content of the drawings and no new matter has been added. Therefore, no marked-up sheets have been included.

Attachment: 6 Replacement Sheets

REMARKS/ARGUMENTS

In this amendment, claims 7, 16, and 23 are amended. Claims 1-6 and 17 are canceled. Thus, after entry of this amendment, claims 7-22 and 24-28 will be pending.

Rejection under 35 U.S.C. § 103(a), Devins, Hartmann, and Steeg

Claims 7-15 are rejected under 35 U.S.C.. 103(a) as being unpatentable over Devins (U.S. 6,615,167) in view of Hartmann (U.S. 6,096,091), and further in view of U.S. Patent No. 5,478,618 to Van de Steeg et al. (hereinafter, "Steeg").

Claims 7-15, 23

Claim 7 is allowable over the cited references, either alone or in combination, as they do not teach or suggest each and every element of claim 7. For example, claim 7 recites:

> *a programmable logic integrated circuit comprising an embedded processor portion and a programmable logic portion, wherein the embedded processor portion includes a watchdog timer circuit; and*
>
> *an external configuration source integrated circuit that is coupled to the programmable logic integrated circuit and that stores configuration information for the programmable logic integrated circuit, wherein when the watchdog timer circuit asserts a triggered signal output due to not reloading the watchdog timer circuit within a timeout period, configuration data is loaded from the external configuration source into the programmable logic integrated circuit.*

Steeg discloses placing a watchdog timer on a first programmable logic circuit 29 for resetting a second programmable logic circuit 37. *See Steeg*, FIG. 2 and col. 8 lines 49-59. The first programmable logic circuit and the second programmable logic circuit are physically and electrically isolated to prevent faults and other noise associated with the second programmable logic circuit from affecting the first programmable logic circuit. *Id.*, col. 3 lines 47-53.

As taught by Steeg, without electrical isolation, circuit interruptions and power losses from the second programmable logic circuit (e.g., the I/O circuit) could damage or disable the watchdog timer circuit (e.g., the controller electronics). *Id.*, FIGS 4 and 5, col. 1 lines 32-37, and col. 8, lines 49-59 . As Steeg requires physical and electrical isolation, Steeg teaches away from placing a watchdog timer and reloading register on the same die. Therefore, it is not

obvious when referring to Steeg to place the *programmable logic portion and the embedded processor portion with a watchdog timer on the same integrated circuit.*

Furthermore, in Steeg, a reset/clear signal is sent to the send logic circuit 39; however, Steeg does not say what the outcome is. *Id.*, col. 8 lines 49-59. Even if the effect is to load configuration data, the loading would occur from 2nd configuration file 38 within second logic circuit 37. *Id.*, FIG. 2 and col. 4 lines 31-34. Thus, even if configuration data would be loaded, Steeg does not teach or suggest the configuration data is loaded from an "*external configuration source integrated circuit*," as recited by claim 7.

Additionally, it is only the second logic circuit 37 that is reset and not the first logic circuit 29. Thus, even if the 2nd configuration file 38 was to be reloaded, then the configuration data would come from the first logic circuit 29. *Id.*, col. 10 lines 35-45. Accordingly, even if the circuit 27 and 39 were combinable on a single integrated circuit, then the configuration data that is reloaded due to the trigger signal would come from the same integrated circuit and not from an external one.

For at least the reasons stated above, Applicants submit that claim 7 and its dependent claims 8-15 are allowable over the cited references. Applicants submit that claim 23 is also allowable for a similar rationale.

Rejection under 35 U.S.C. § 103(a), Devins, Hartmann, and Yokouchi

Claims 16-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devins in view of Hartmann, and further in view of U.S. Patent No. 4,796,211 to Yokouchi et al. (hereinafter, "Yokouchi").

Claims 16-22, 24-28

Claim 16 is allowable over the cited references, either alone or in combination, as they do not teach or suggest each and every element of claim 16. For example, claim 16 recites:

> wherein triggering of the watchdog timer circuit is avoided when the watchdog timer circuit is periodically reloaded, before a timeout period, by writing a magic value to a reload register, and wherein loading a value other than the magic value also causes the watchdog timer circuit to generate a triggered signal.

At page 9, the Office Action states that neither Devins nor Hartmann teach the claimed limitation of the watchdog timer being triggered if a count register of the timer is permitted to count to a final value before the count register is reloaded.

The Office Action also states that Yokouchi discloses a watchdog timer with a reset detection circuit (see Fig. 1) that indeed includes the timer being triggered if the count register is permitted to count to a final value before the count register is reloaded (in this case the final value is 16 ms - see Yokouchi, col. 1, 11. 36 - 47).

However, Yokouchi does not mention a trigger signal being generated because of loading a value other than the magic value, as recited in claim 16. Support for this amendment can be found at least in paragraphs 15 and 72.

For at least the reasons stated above, Applicants submit that claim 16 and its dependent claims 17-22 and 24-28 are allowable over the cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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Attachments
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